CLAIM AMENDMENTS:

Claim 1 (Currently Amended): A semiconductor device having a semiconductor substrate formed with a plurality of electrode pads, and wiring electrically connecting said electrode pads to external electrodes to be connected to conductive patterns formed on an external circuit board, said wiring formed ~~in~~ as a plurality of layers, said semiconductor device comprising:

insulating layers interposed between the layers of said wiring, and between ~~the~~ a lowermost layer of said wiring and said semiconductor substrate, thereby to ensure insulation therebetween;

each of said layers of said wiring ~~each~~ having depressed portions located at via holes formed in said insulating layers, said depressed portions being connected to the ~~lower~~ lowermost layer of said wiring or said electrode pads, and having flat portions located on said insulating layers and serving as lateral conductors to other electrical connections on said insulating layers;

bump electrodes formed on said depressed portions of ~~the~~ an uppermost layer of said wiring;

external electrodes formed on the top surfaces of said bump electrodes; and

a sealing layer formed over said uppermost layer of said wiring so as to expose the top surface of said bump electrodes.

Claim 2 (Original): A semiconductor device according to claim 1, wherein said depressed portions of said layers of said wiring including said uppermost layer are formed in positions where said depressed portions overlap with each other.

Claim 3 (Currently Amended): A semiconductor device according to claim 1, wherein each of said bump electrodes is formed so as to ~~erect~~ rise from a bottom portion of the corresponding depressed portion.

Claim 4 (Original): A semiconductor device according to claim 1, wherein each of said bump electrodes is formed so as to cover the corresponding depressed portion.

Claim 5 (Currently Amended): A semiconductor device according to ~~claim 1,~~ claim 1, wherein an uppermost insulating layer is further formed between said sealing layer and said uppermost layer of said wiring, said uppermost insulating layer having a substantially flat surface and does not include a filler material.

Claim 6 (Original): A semiconductor device according to claim 1, further comprising seed layers each formed under the corresponding layer of said wiring and acting as an electrode for forming the corresponding layer of said wiring.

Claim 7 (Currently Amended): A semiconductor device according to claim 6, wherein said seed layer has an opening at each of said depressed portions of said wiring.

Claim 8 (Currently Amended): A semiconductor device according to claim 6, wherein said seed ~~layers~~ layers, except ~~the~~ a seed layer formed under said lowermost layer of said ~~wiring~~ wiring, are made of a material that is the same as that of said wiring.

Claim 9 (Currently Amended): A semiconductor device according to claim 1, wherein each of said external electrodes is made of a solder material including tin, and each of said bump electrodes is made of ~~copper, and~~ copper; further comprising

a barrier layer including nickel ~~is~~ formed between each of said external electrodes and the corresponding bump electrode.

Claim 10 (Original): A semiconductor device according to claim 1, wherein, assuming that distances from a neutral point of a thermal stress of the semiconductor device to an arbitrary pair of bump electrodes among said bump electrodes are set as L1 and L2, and heights of said pair of bump electrodes are set as H1 and H2, the heights of said pair of bump electrodes are determined so

as to satisfy:

when L1<L2, then H1≤H2.

Claim 11 (Currently Amended): A semiconductor ~~device~~ device, comprising:

a semiconductor substrate which has a main surface;

an electrode pad which is formed on the main surface;

an insulating layer;

a plurality of redistribution wirings which are formed over the main surface and which are formed at different levels, wherein the redistribution wiring at a lowermost level is connected to the electrode pad, ~~and~~ wherein the redistribution wiring at an uppermost level is disposed on the insulating layer and has a depressed portion to which the redistribution wiring at the ~~lower~~ lowermost level is connected, and flat portions located on said insulating layers and serving as lateral conductors to other electrical connections on said insulating layers;

a bump electrode which is formed on the depressed portion of the redistribution wiring at the uppermost level;

an external electrode which is formed on ~~the~~ a top surface of the bump electrode; and

a sealing layer which is formed over the redistribution wiring at the uppermost level so as to expose the top surface of the bump electrode.

Claim 12 (Currently Amended): A semiconductor device according to claim 11, wherein the redistribution wiring at the ~~lower~~ lowermost level has a depressed portion and wherein the depressed portion of the redistribution wiring at the uppermost level and the depressed portion of the redistribution wiring at the ~~lower~~ lowermost level are positioned to overlap each other.

Claim 13 (Currently Amended): A semiconductor device according to claim 11, wherein the bump electrode is formed so as to ~~erect~~ rise from a bottom portion of the depressed portion.

Claim 14 (Currently Amended): A semiconductor device according to claim 11, wherein the bump electrode is formed so as to entirely cover the depressed portion ~~entirely~~.

Claim 15 (Currently Amended): A semiconductor device according to claim 11, further comprising ~~an~~ a further insulating layer which is formed between the sealing layer and the redistribution wiring at the uppermost level and which has a substantially flat surface and does not include a filler material.

Claim 16 (Currently Amended): A semiconductor ~~device~~ device, comprising:

a semiconductor substrate which has a main surface;

a plurality of electrode pads which are formed on the main surface;

a plurality of redistribution wirings which are formed over the main surface and which are formed at different levels, wherein the redistribution wirings at a lowermost level are connected to corresponding electrode pads and the redistribution wirings at an uppermost level are coupled to corresponding redistribution wirings at the lowermost levels through redistribution wirings at a middle level;

a plurality of bump electrodes which are formed on corresponding portions of the redistribution wirings at the uppermost level;

a plurality of external electrodes which are formed on ~~the~~ a top surface of corresponding bump electrodes; and

a sealing layer which is formed over the redistribution wirings at the uppermost levels so as to expose the top surface of the bump electrodes,

wherein assuming that distances from a neutral point of a thermal stress of the semiconductor device to an arbitrary pair of bump electrodes among the bump electrodes are set as L1 and L2, and a length of the pair of bump electrodes are set as H1 and H2, the length of the pair of bump electrodes are determined so as to satisfy:

when $L1<L2$, then $H1 \leq H2$.

Claim 17 (Currently Amended): A semiconductor ~~device~~ device, comprising:

a semiconductor substrate which has a main surface;

an electrode pad which is formed on the main surface;

a plurality of insulating layers which are formed over the main surface, and which are formed at different levels and which have via holes;

a plurality of redistribution wirings which are formed at different levels, the redistribution wiring at each level being formed on a surface and the via hole of a corresponding insulating layer, wherein the redistribution wiring at a lowermost level is connected to the electrode pad, ~~and~~ wherein the redistribution wiring at an uppermost level has a depressed portion located at the via hole defined by the insulating layer at the uppermost level and is connected to the redistribution wiring of the ~~lower~~ lowermost level at the via hole, and has flat portions located on said insulating layers and serving as lateral conductors to other electrical connections on said insulating layers;

a bump electrode which is formed on the depressed portion of the redistribution wiring at the uppermost level;

an external electrode which is formed on ~~the~~ a top surface of the bump electrode; and

a sealing layer which is formed over the redistribution wiring at the uppermost level so as to expose the top surface of the bump electrode.

Claim 18 (Currently Amended): A semiconductor device according to claim 17, wherein the redistribution wiring at the ~~lower~~ lowermost level has a

depressed portion located at the via hole of the insulating layer at the ~~lower~~ lowermost level and wherein the via hole of the insulating layer at the uppermost level and the via hole of the insulating layer at the ~~lower~~ lowermost level are positioned to overlap each other.

Claim 19 (Currently Amended): A semiconductor device according to claim 17, wherein the bump electrode is formed so as to ~~erect~~ rise from a bottom of the via hole.

Claim 20 (Currently Amended): A semiconductor device according to claim 17, wherein the bump electrode is formed so as to entirely cover the via hole ~~entirely~~.